

Profile: Dr. Sanjeev Manhas



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Assistant Professor

Semiconductor Devices and VLSI Technology (SDVT)

Dept of Electronics & Computer Engineering

IIT Roorkee, Uttarakhand, India 247667

Tel: +91-1332-28 5147 (O), +91-9760511774 (M)

Email: samanfec@iitr.ernet.in, smanhas2000@yahoo.com

Research Interests

- Silicon nano-wire circuit design, parasitic evaluation and fabrication technologies
- Nano-scale MOSFET modeling and reliability
- VLSI technologies
- DRAM leakage mechanisms and refresh
- Organic thin film transistors

Courses offered

- EC242 – Semiconductor devices and technology
- EC555 – VLSI technology
- EC551 – Device modeling for circuit simulation

Academic Background

- M. Sc. (Panjab University Chandigarh, India) 1993
- M Tech (IIT Madras, India) 1995
- PhD (De Montfort University, Leicester, UK) 2003

Work Experience

Position	Organization	From	To
Assistant Professor	IIT Roorkee, India	Aug-08	To date
Sr. Research Scientist	Institute of Microelectronics, Singapore	Sep-07	Aug-08
Member Technical Staff	Tech Semiconductor, Singapore	Jan-03	Aug-07
Research Fellow	De Montfort University Leicester, UK	Apr-01	Dec-02

Honors, Awards and Memberships

- Microelectronics Reliability best paper award for work on “the nature of hot carrier damage in LDD MOSFETs” Aug 2002
- Reviewer IEEE electron device letters 2000-2002
- Member IEEE since January 2000
- Graduate Aptitude Test in Engineering (GATE) scholarship (1993)
- Indian National Research Scholarship (CSIR, 1993)
- State (Himachal Pradesh, India) graduate merit award (1991)

Research and Development Projects

1. Design and analysis of Si Nano-wire CMOS based Memory and logic circuits for low power applications, Indian Institute of Technology, Roorkee, Dec 08 -

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2. **Development of stringer free Si nanowire MOSFET technology for parasitic free Si nanowire circuit fabrication**, Institute of Microelectronics, Singapore, Sept 2007- July 2008
3. Developed reliable Cu plug process technology for sub 100nm technology nodes, Institute of Microelectronics, Singapore, Jan 2008 – Sept 2008
4. **Transistor module Technology Transfer of 115nm, 110nm and 90nm 8F2/6F2 DRAM Technologies** in collaboration with Micron Technology Boise, Idaho USA, 2004-2007
5. **Development of reliable Cell to Cell short free process for 78nm Double Sided Container 1Gb DRAM Process Technology**, Tech Semiconductor, Singapore, Jan 2007- June 2007
6. **Gate Stack Stress Optimization and Technology Transfer of sub 100nm DRAM Technology**, Tech Semiconductor, Singapore, Jan 2006-July 2006
7. Development of gate reticle for reduced standby leakage and improved reliability, Tech Semiconductor, Singapore, Jan 2006 – Dec 2006
8. **Design and Optimization of Stop On Oxide Gate Nitride Spacer Etch Process Technology for Retention Time Improvement in 110nm DRAM Process Technology**, Tech Semiconductor, Singapore, Jan 2004 - June 2004
9. **Early Stage Hot Carrier Degradation in State-of-the-art Deep Submicron Semiconductor Devices**. Developed a new model to describe evolution of hot carrier damage in deep submicron MOSFETs, De Montfort University, Leicester UK, 1999-2001.
10. Study of effect of radiation on MOS capacitors fabricated on SOI substrates Indian Institute of Technology, Madras, India, June 1995- Dec 1995

M. Tech. and Ph.D. Students

PhD

1. Gaurav Koushal, E&CE IIT Roorke, Si Nano-wire based memory design and simulation, Dec 2008 -

Graduate

1. **Chen Min Cong**, Electrical and electronic Engineering, Nanyang Technical University/ASTAR Institute of Microelectronics, Singapore, Copper plug process development for sub 100nm CMOS technology, Aug 2007 – Sep 2008
2. **RANJIT CHAKRAPANI RAVI**, Electrical and electronic Engineering, Nanyang Technical University/ASTAR Institute of Microelectronics, Singapore, FABRICATION OF STRINGER-FREE 0.13 μ m MOSFETs, Jan 2008- Jul 2008
3. **Atul Kumar**, Semiconductor Devices and VLSI Technology (SDVT), Dept of Electronics & Computer Engineering, IIT Roorkee
4. **Kumar NVSS**, Semiconductor Devices and VLSI Technology (SDVT), Dept of Electronics & Computer Engineering, IIT Roorkee, STRAIN SILICON for sub 100nm VLSI Technologies, Sept. 2008 -
5. **Vevek Harshey**, Semiconductor Devices and VLSI Technology (SDVT), Dept of Electronics & Computer Engineering, IIT Roorkee, SILICON-ON-INSULATOR GATE- ALL-AROUND DEVICES, Sept. 2008 -
6. **Sravan Sreeram**, Semiconductor Devices and VLSI Technology (SDVT), Dept of Electronics & Computer Engineering, IIT Roorkee, High-k/Metal Gates for High-Volume Manufacturing, Sept. 2008 -

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List of Publications

1. N Singh, K D. Buddharaju, **S. K. Manhas**, A. Agarwal, S C. Rustagi, G. Q. Lo, N. Balasubramanian, "Si, SiGe Nano-wire Devices by Top-Down Technology and Their Applications," IEEE Transactions on Electron Devices, Vol. 55, No. 11, p. 3107, 2008.
2. M. M. De Souza, **S. K. Manhas**, D. Chandra Sekhar, A. S. Oates, P. Chaparala, "Influence of Mobility model on extraction of stress dependent source-drain series resistance", Microelectronics Reliability, 25, Vol 44, Jan 2004
3. G. Cao, **S. K. Manhas**, E.M.S. Narayanan, M. M. De Souza, D. Hinchley, "Comparative study of drift region designs in RF LD MOSFETs", IEEE Trans Electron Devices, Vol 51, Issue 8, Aug. 2004, 1296 – 1303
4. **S. K. Manhas**, D. Chandra Sekhar, A. S. Oates M. M. De Souza, "Characterisation of Series Resistance Degradation through Charge Pumping Technique", Microelectronics Reliab., Vol. 43, p. 617, 2003
5. **S. K. Manhas**, M. M. De Souza, A. S. Oates, "Quantifying the Nature of Hot Carrier Degradation in the Spacer Region of LDD nMOSFETs," IEEE Transactions on Device and Materials Reliability, vol. 1, no. 3, p. 134, Sept. 2001
6. M. M. De Souza, J. Wang, **S. Manhas**, E. M. Sankara Narayanan, A.S. Oates, "A Comparison of Early Stage Hot Carrier Degradation Behaviour in 5 and 3 V Sub-micron Low Doped Drain Metal Oxide Semiconductor Field Effect Transistors," Microelectronics Reliab., Vol. 44, No. 2, p. 169, Feb. 2001.
7. **S. K. Manhas**, M. M. De Souza, A. S. Oates, Y. Chen, "A New Extraction Methodology for Series Resistance and Mobility Degradation of Hot Carrier Stressed N-MOSFETs," (unpublished)
8. **S. K. Manhas**, M Chen, K D Buddharaju, H Y Li, R Murthy, S Balakumar, N Singh, G Q Lo and D L Kwong, "Copper Plug Barrier Process Optimization for Reliable Transistor Performance," International Symp on Solid State Circuits and Materials (SSDM 2008), 23 - 26 Sep, p. 390, 2008, Japan.
9. N. Balasubramanian, N. Singh, S.C. Rustogi, K.D. Buddharaju, J. Fu, Z. Hui, S. Balakumar, A. Agarwal, **S.K. Manhas**, G.Q.Lo, and D.L. Kwong, "Si Nano-wire CMOS Transistors and Circuits by Top-Down Technology Approach," 213th Electrochemical Soc. Meet., Phoenix, May 18-22, 2008
10. H. Zhao, S.C. Rustagi, N. Singh, F.-J. Ma, G.S. Samudra, K.D. Budhaaraju, **S. K. Manhas**, C.H. Tung, G.Q. Lo, G. Baccarani, "Sub-Femto-Farad Capacitance-Voltage Characteristics of Single Channel Gate-All-Around Nano Wire Transistors for Electrical Characterization of Carrier Transport," Proc IEEE Int Electron Devices Meet, Dec 15-17, San Francisco, 2008
11. **S. K. Manhas**, M. M. De Souza, A. O. Oates, S. C. Chetlur, E. M. Sankara Narayanan, "Early Stage Hot Carrier Degradation of State-of-the-art LDD N-MOSFETs," Proc. IEEE Intl. Reliability Physics Symposium (IRPS), p. 108, April 2000.
12. **S. K. Manhas**, D. C. Chandrasekhar, M. M. De Souza, A. S. Oates, "Nature of Hot Carrier Damage in Spacer Oxide of LDD n-MOSFETs," Proc. 23rd International Conference on Microelectronics, p. 735, Nis, Yugoslavia, May 2002 (Microelectronics Reliability Best Paper Award).
13. **S. K. Manhas**, M. M. De Souza, A. S. Oates, "Impact of Oxide Degradation on Universal Mobility Behaviour of n-MOS Inversion Layers", Proc. 9th Int'l Symposium on the Physical & Failure Analysis of Ics (IFPA), p. 227, July 2002, Singapore.
14. M. M. De Souza, G. Cao, E. M. Sankara Narayanan, F. Youming, **S. K. Manhas**, J. Luo, N. Moguilnaia,, "Progress In Silicon RF Power MOS Technologies—Current And Future Trends.," 4th

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IEEE International Caracas Conference on Devices, Circuits and Systems (ICDCS), April 2002, Aruba, Dutch Caribbean.

15. M. Mugnier, **S. K. Manhas**, D. Chandra Sekhar, Krishnan, R. Cross, E. M. Sankara Narayanan, M. M. De Souza, "Degradation Behaviour of Polysilicon High Voltage Thin Film Transistors," Proc. 9th Int'l Symposium on the Physical & Failure Analysis of Ics (IFPA), p. 219, July 2002, Singapore.
16. **S. K. Manhas**, M.M. De Souza, D. Chandra Sekhar, E.N. Sankara Narayanan "Hot carrier degradation of deep submicron LDD N-MOS technologies" PREP 2002 Proceedings, Electronics Track, Vol. 2, University of Nottingham, UK
17. D. Chandra Sekhar, **S.K. Manhas**, E.M.S. Narayanan, Y. Chen, A.S. Oates, M.M. De Souza, "Hot-carrier degradation of ultrathin oxide pMOSFETs", PREP 2002 Proceedings, Electronics Track, Vol. 1, University of Nottingham, UK
18. **S. K. Manhas**, Joel Koh, Poh Keng Wah, Anthony Lee , "Decoupled Plasma Nitridation for Deep Submicron Process Technology," Proc. 8th Tech seminar on process technology, 29-30th June 2003, Singapore
19. **S. K. Manhas**, William Chia, Alex Lee, Anthony Lee, Devesh K Datta, S. Krishnan, "Design and Optimization of Stop On Oxide Gate Nitride Spacer Etch Process for Retention Time Improvement in 0.11um DRAM Process Technology", Proc., 9th Tech seminar on process technology, 29-30th 2004, Singapore.
20. **S. K. Manhas**, Arvind Kumar, Terence Kek, "Gate Stack Stress Optimization in sub 100nm DRAM Technology," Proc., 10th Tech seminar on process technology, 29-30th June 2006, Singapore.
21. **S. K. Manhas**, M. Yhoz Hendryanto, Thong Chee Meng, Devesh Dutta, "A Study of Anomalous Cell to Cell Short in 78nm Double Sided Container 1Gb DRAM Process Technology," Proc., 11th Tech seminar on process technology, 2-3rd August 2007, Singapore.
22. Devesh Dutta, **S. K. Manhas**, Chong Hui Chin, Teo Teck Hock, "Optimization of Capacitor Top Cell Plate Process for 1Gb DRAM Technology," Proc., 11th Tech seminar on process technology, 2-3rd August 2007, Singapore.